In the Claims:

1. (currently amended) In a semiconductor die having an op-amp, a method of reducing package stress, which comprises the steps ~~act~~ of:

providing a semiconductor chip;

locating the centroid of the semiconductor chip; and

~~placing~~ forming an op-amp having matched components in said semiconductor chip, the input stages of said matched components of the op-amp spaced apart and disposed at substantially the centroid of the semiconductor chip ~~in a region of the die having the least stress gradients~~.

2. (previously presented) The method according to clam 1, wherein the region is substantially in the center of the die.

3. (canceled).

4. (previously presented) The method according to clam 1, wherein the matched components are current mirror input stages of the op-amp.

5. (previously presented) The method according to clam 1, wherein the op-amp is one of a single, dual, and quad op-amp.

6. (previously presented) The method according to clam 1, wherein the op-amp is a differential op-amp.

7. (canceled)

8. (previously presented) The method according to clam 1, which further comprises:

disposing gain stages of the op-amp in an intermediate region of the die.

9. (previously presented) The method according to clam 1, which further comprises:

disposing output stages of the op-amp in an outer region of the die.

10-13 (canceled).

14. (currently amended) A semiconductor configuration, comprising:

a die having a centroid; ~~region with the least stress gradients~~ and

an op-amp in said die, said op-amp containing matched components having inputs, said inputs spaced apart and disposed at substantially said centroid ~~substantially in said region~~.

15. (previously presented) The semiconductor configuration according to clam 14, wherein said region is substantially in the center of the die.

16. (canceled)

17. (previously presented) The semiconductor configuration according to clam 14, wherein said matched components are current mirror input stages

18. (previously presented) The semiconductor configuration according to clam 14, wherein said op-amp is one of a single, dual, and quad op-amp.

19. (previously presented) The semiconductor configuration according to clam 14, wherein said die includes an intermediate region having gain stages.

20. (previously presented) The semiconductor configuration according to clam 14, wherein said die includes an outer region having output stages.

21. (new) In a semiconductor device, a method of reducing package stress, which comprises the steps of:

providing a semiconductor chip;

locating the centroid of the semiconductor chip; and

forming a device having matched components in said semiconductor chip, the input stages of said matched components spaced apart and disposed at substantially the centroid of the semiconductor chip.

22. (new) The method according to clam 21, wherein the region is substantially in the center of the die.

23. (new) A semiconductor configuration, comprising:

a die having a centroid: and

an op-amp in said die, said op-amp containing matched components having inputs, said inputs spaced apart and disposed at substantially said centroid .

24. (new) The semiconductor configuration according to clam 23, wherein said region is substantially in the center of the die.

25. (new) The semiconductor configuration according to claim 21 wherein said device is an analog circuit.

26. (new) The semiconductor configuration according to claim 22 wherein said device is an analog circuit.

27. (new) The semiconductor configuration according to claim 23 wherein said device is an analog circuit.

28. (new) The semiconductor configuration according to claim 24 wherein said device is an analog circuit.